WHAT IS CLAIMED IS:

1   1.   A digital-to-analog converter to convert into an analog quantity a digital code

2   including a first part of more significant bits and a second part of less significant bits,

3   comprising:

4   a first section to convert the first part of the digital code into a first voltage, said

5   first voltage being of discrete voltages that are integral multiples of a predetermined first voltage

6   step;

7   a second section to convert the second part of the digital code into a current;

8   means for transforming the current of the second section into a second voltage,

9   said second voltage being of discrete voltages that are integral multiples of a second voltage step

10 equal to 1/2L of the product of the first voltage step multiplied by a predetermined coefficient,

11 where L is the number of the less significant bits of the digital code to be converted;

12   control means of the first and the second section; and

13   summation means for generating the analog quantity as the sum of the second

14 voltage and the product of the first voltage multiplied by the predetermined coefficient,

15 comprising a summation circuit with resistive feedback means including a voltage divider; and

16   wherein the means for transforming the current into a second voltage comprises a

17 conversion resistor that forms part of the voltage divider.

1   2.   The converter in accordance with Ciaim 1, wherein

2   the summation circuit comprises an operational amplifier having a first input, a

3   second input and an output connected to the converter output;

4   the predetermined coefficient is the gain of the operational amplifier;

5   the voltage divider of the resistive feedback means is connected between the

6   output and the first input of the operational amplifier;

7   the first section comprises a resistive network having 2M taps, where M is the

8   number of the more significant bits of the digital code to be converted, and substantially equal

9   resistances between adjacent taps, and 2M electronic switches each inserted between a respective

10   tap and a common node connected to the second input of the operational amplifier;

11   the second section comprises a group of L current generators presented in binary

12   form, selection means of the L current generators and means for conveying the current of the

13   selected generators onto a common node connected to the conversion resistor; and

14   the control means comprise means for selectively operating the electronic

15   switches in such a way as to individually connect each of the 2M taps to the second input of the

16   operational amplifier according to the first part of the digital code and means for selectively

17   operating the selection means of the current generators according to the second part of the digital

18   code.

1   3.   The converter in accordance with Claim 2, wherein the second section comprises

2   a further group of L current generators presented in binary form and further selection means of

3   the L further current generators and wherein the control means comprise a selection logic that

4   alternatively activates the use of either one or the other group of generators according to whether

5   the digital code to be converted does or does not exceed, respectively, a predetermined value.

1   4.   The converter in accordance with Claim 1, wherein

2   the summation circuit comprises an operational amplifier having a first input, a

3   second input and an output connected to the output of the converter;

4   the predetermined coefficient is the gain of the operational amplifier;

5   the voltage divider of the resistive feedback means is connected between the

6   output and the first input of the operational amplifier;

7   the first section comprises a resistive network having 2M-1 taps, where M is the

8   number of the more significant bits of the digital code to be converted, and substantially equal

9   resistances between adjacent taps, and 2M-1 electronic switches, each inserted between a

10   respective tap and a common node connected to the second input of the operational amplifier;

11   the second section comprises a group of L current generators presented in binary

12   form, selection means of the L current generators, a further group of current generators, of which

13   L are presented in binary form and one complementary generator having the same weight as the

14   generator of smallest weight of the L current generators, further selection means of the further

15   group of current generators and means for conveying onto a common node, connected to the

16   conversion resistor, the current of the selected generators;

17   the control means comprise means for selectively operating the electronic

18   switches in such a way as to individually connect each of the 2M-1 taps to the second input of

19   the operational amplifier according to the first part of the digital code, means for selectively

20   operating the selection means of the current generators according to the second part of the digital

21   code and a selection logic that alternatively activates the use of one or the other group of

22   generators according to whether the digital code to be converted does or does not exceed,

23   respectively, a predetermined value.

1   5.   The digital-to-analog converter in accordance with Claim 4, wherein the

2   electronic switches of the first section form a first and a second group of electronic switches

3   having an electronic switch in common and wherein the selection logic determines the operation

4   of the electronic switches of the first or the second group according to whether the digital code to

5   be converted does or does not exceed, respectively, a predetermined value and determines the

6   permanent selection of the complementary generator of the further group of current generators

7   when the digital code to be converted does not exceed the predetermined value.

1   6.   A converter in accordance with Claim 5, wherein the further current generators of

2   the second group comprise P-channel MOS transistors.

1   7.   The converter in accordance with Claim 4, wherein the predetermined value is

2   expressed by the digital code having the most significant bit equal to 0 and the remaining bits

3   equal to 1.

1   8.   The converter in accordance with Claim 4, wherein the current generators of the

2   second group comprise N-channel MOS transistors.

1   9.   A converter in accordance with Claim 3, wherein the further current generators of

2   the second group comprise P-channel MOS transistors.

1   10.   A digital-to-analog converter to convert into an analog quantity a digital code of L

2   bits, comprising

3   a first group of L current generators presented in binary form;

4   first selection means of the L current generators;

5   means for conveying onto a common output node the current of the selected

6   generators;

7   control means to selectively operate the selection means according to the digital

8   code of L bits comprising:

9   a second group of L current generators presented in binary form and

10   second selection means of the second group of L current generators and in that

11   the control means comprise a selection logic that alternatively activates the

12   use of the first or the second group of generators according to whether the digital code to be

13   converted does or does not exceed, respectively, a predetermined value.

1   11.   The converter in accordance with Claim 10, wherein the predetermined value is

2   expressed by the digital code having the most significant bit equal to 0 and the remaining bits

3   equal to 1.

1   12.   The converter in accordance with Claim 10, wherein the current generators of the

2   first group comprise N-channel MOS transistors and the current generators of the second group

3   comprise P-channel MOS transistors.

1   13.   A circuit, comprising:

2   a more significant bit converter having an analog voltage output indicative of a

3   more significant bit portion of an input digital signal;

4   a less significant bit converter having an analog current output indicative of less

5   significant bit portion of the input digital signal;

6   a summation circuit including a first input terminal coupled to the analog voltage

7   output and a second input terminal; and

8   a feedback path comprising a first and second resistor connected to each other at a

9   node to form a series voltage divider, the feedback path coupled between the second input

10   terminal and an output of the summation circuit, the node in the feedback path being connected

11   to the analog current output.

1   14.   The circuit of claim 13 wherein the output of the summation circuit produces an

2   analog voltage signal which is a conversion of the input digital signal.

1   15.   The circuit of claim 13 further including a resistor connected between the second

2   input terminal and a reference voltage.

1   16.   The circuit of claim 15 wherein the summation circuit comprises an operational

2   amplifier circuit.

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1   17.   The circuit of claim 13 wherein the less significant bit converter comprises:

2   a first plurality of current generators; and

3   a selection circuit that selectively connects one or more of the first plurality of

4 current generators to the node in the feedback path based on the less significant bit portion of the

5 input digital signal.

1   18.   The circuit of claim 17 further comprising a current mirror circuit that mirrors, for

2 use by the first plurality of current generators, a current which is flowing in the more significant

3 bit converter.

1   19.   The circuit of claim 13 wherein the less significant bit converter comprises:

2   a first plurality of current generators;

3   a second plurality of current generators; and

4   a selection circuit that selectively connects one or more of the first plurality of

5 current generators to the node in the feedback path, or alternatively selectively connects one or

6 more of the second plurality of current generators to the node in the feedback path, based at least

7 in part on the less significant bit portion of the input digital signal.

1   20.   The circuit of claim 19 wherein the selection circuit chooses between connection

2 of the first and second plurality of current generators based on the more significant bit portion of

3 the input digital signal.

1   21.   The circuit of claim 19 further comprising a current mirror circuit that mirrors, for

2   use by the first and second plurality of current generators, a current which is flowing in the more

3   significant bit converter.

1   22.   A circuit, comprising:

2   a more significant bit converter having an analog voltage output indicative of a

3   more significant bit portion of an input digital signal;

4   a less significant bit converter having an analog current output indicative of less

5   significant bit portion of the input digital signal;

6   a summation circuit including a first input terminal coupled to the analog voltage

7   output and a second input terminal; and

8   a feedback path coupled between the second input terminal and an output of the

9   summation circuit and connected to the analog current output;

10   wherein the less significant bit converter comprises:

11   a first plurality of current generators;

12   a second plurality of current generators; and

13   a selection circuit that selectively connects one or more of the first

14   plurality of current generators to the analog current output, or alternatively selectively connects

15   one or more of the second plurality of current generators to the analog current output, based at

16   least in part on the less significant bit portion of the input digital signal.

1   23.   The circuit of claim 22 wherein the selection circuit chooses between connection

2   of the first and second plurality of current generators based on the more significant bit portion of

3   the input digital signal.

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1 24. The circuit of claim 22 further comprising a current mirror circuit that mirrors, for

2 use by the first and second plurality of current generators, a current which is flowing in the more

3 significant bit converter.

1 25. The circuit of claim 22, wherein the feedback path comprises a first and second

2 resistor connected to each other at a node to form a series voltage divider, the node in the

3 feedback path being connected to the analog current output.